

Appl. No. To Be Assigned; Filed: Herewith
 Dkt. No. 1875.5630000; Group Art Unit: To Be Assigned
 Inventors: Amirichimeh *et al.*; Tel.: (202) 371-2600
 Title: System and Method of Phase-Locking a Transmit Clock
 Signal Phase with a Receive Clock Signal Phase

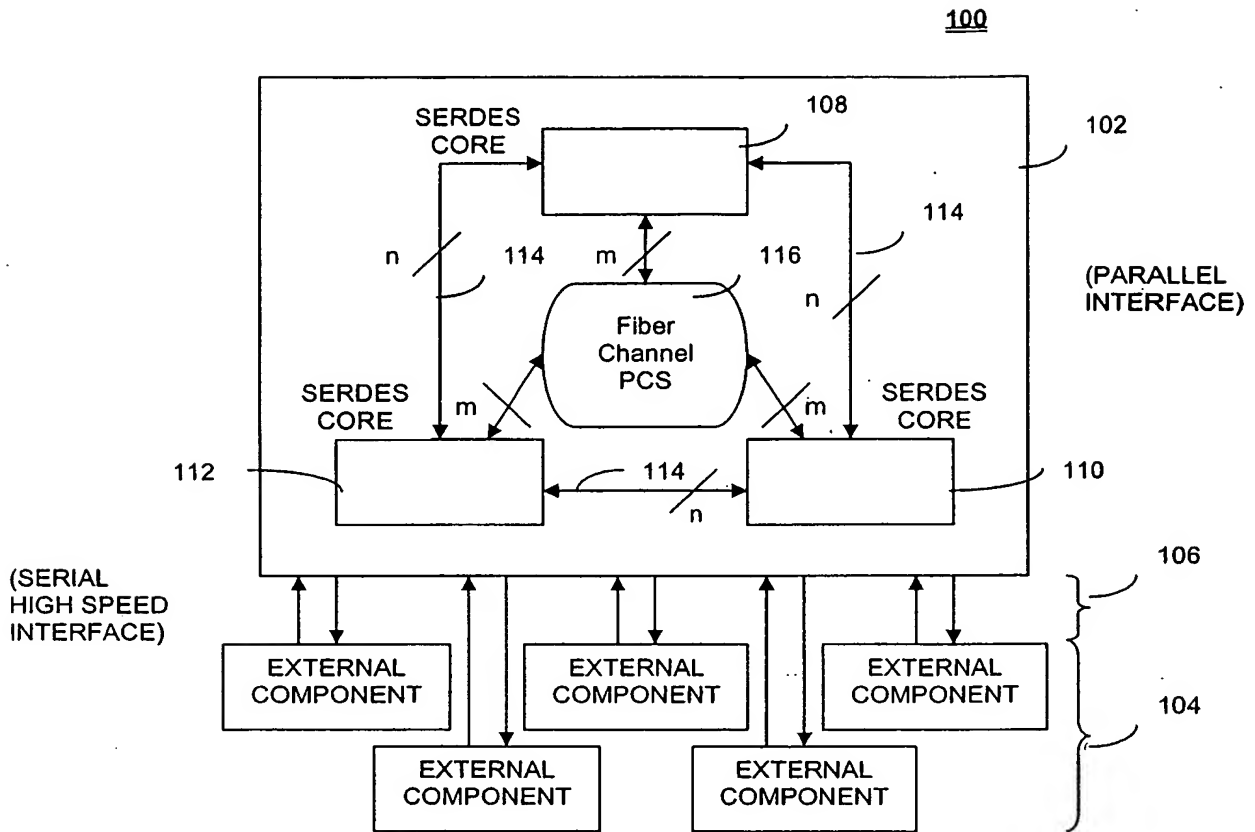


FIG. 1

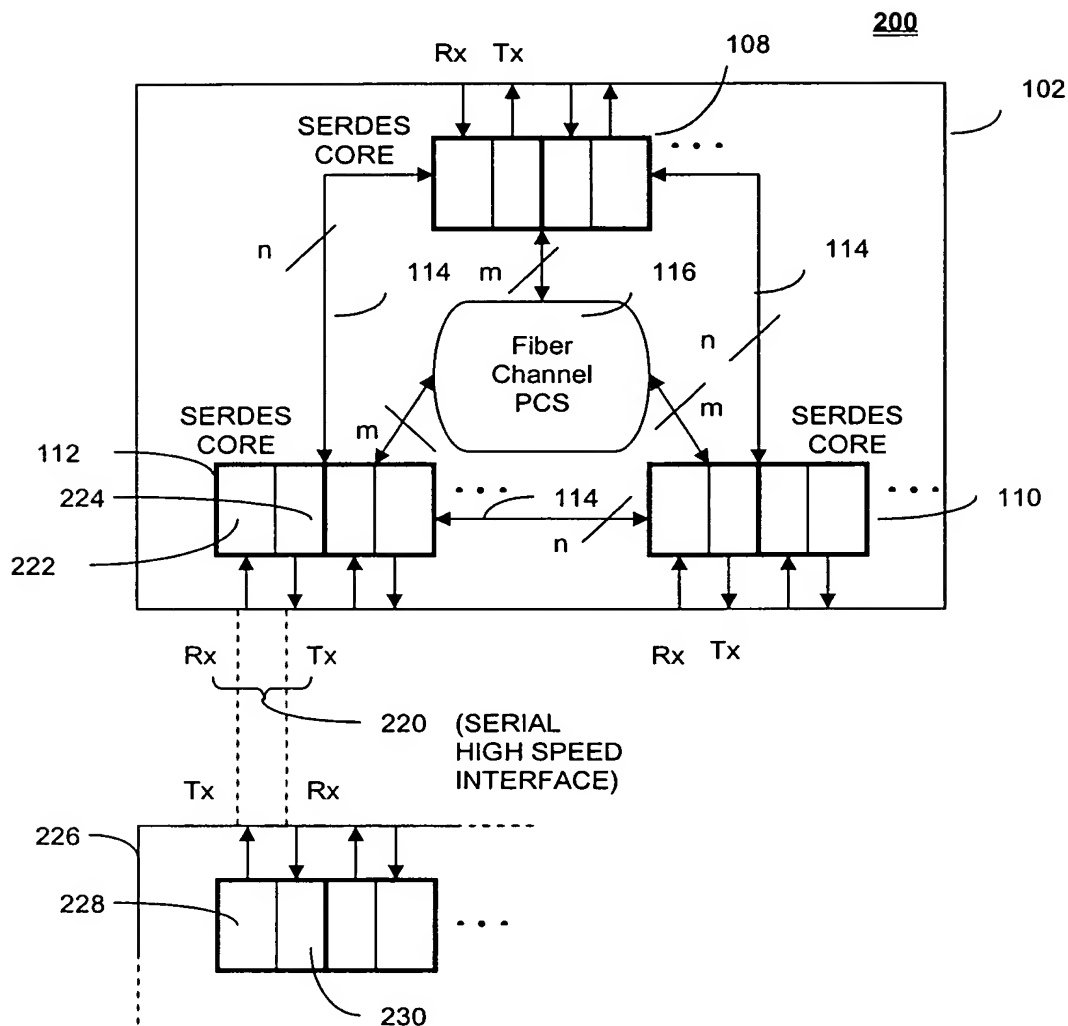


FIG. 2

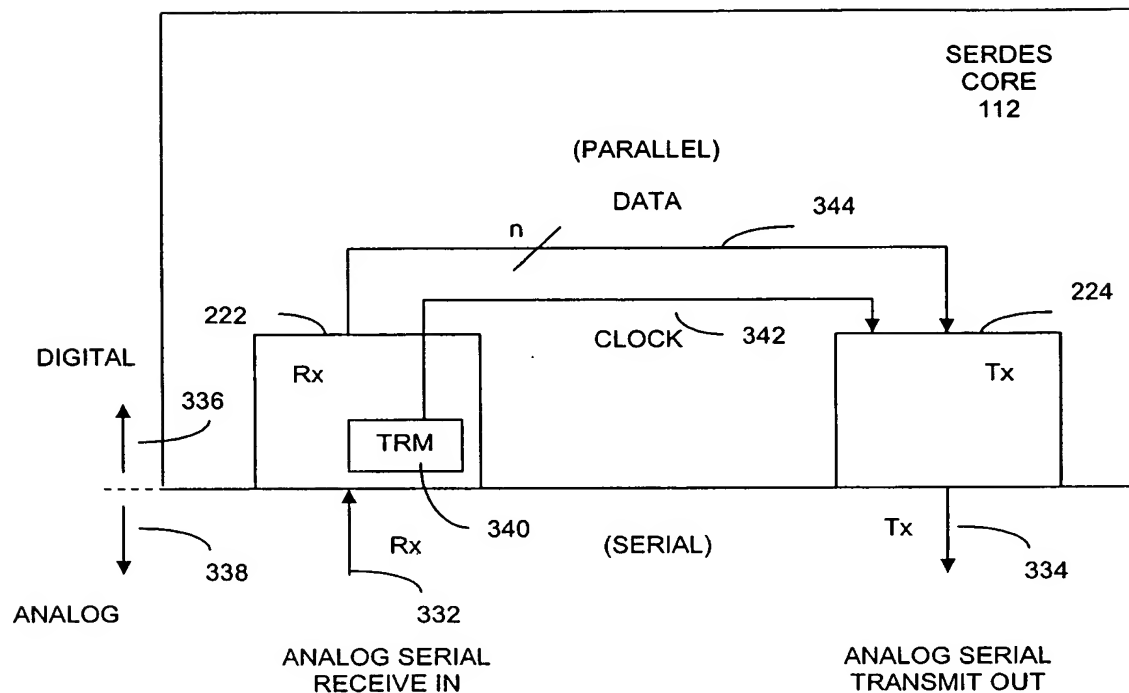


FIG. 3

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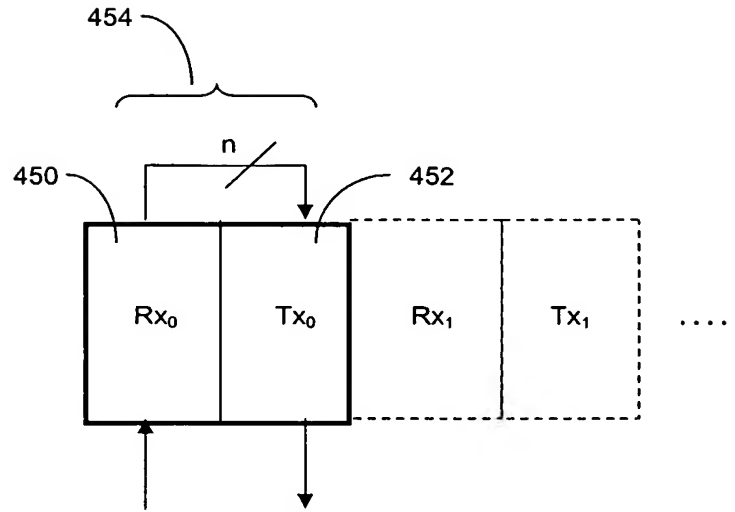


FIG. 4
(INTRALANE)

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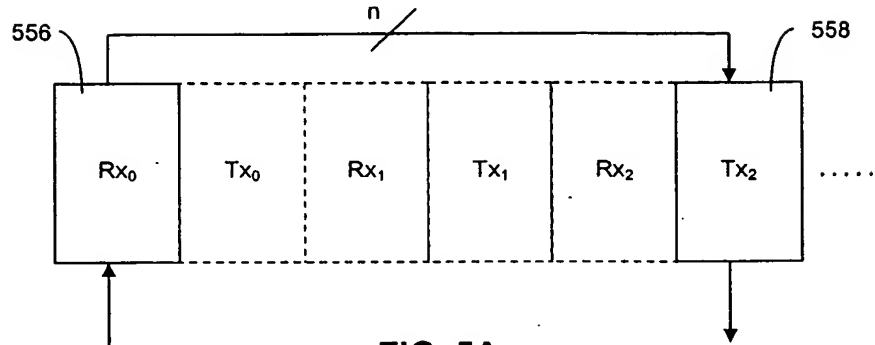


FIG. 5A
(INTERLANE)

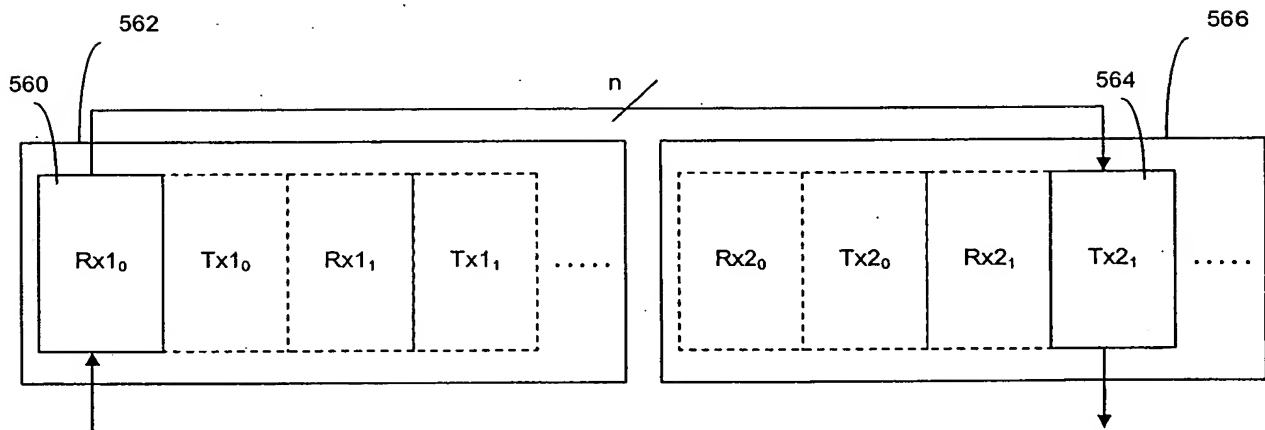


FIG. 5B
(INTERLANE / INTERCORE)

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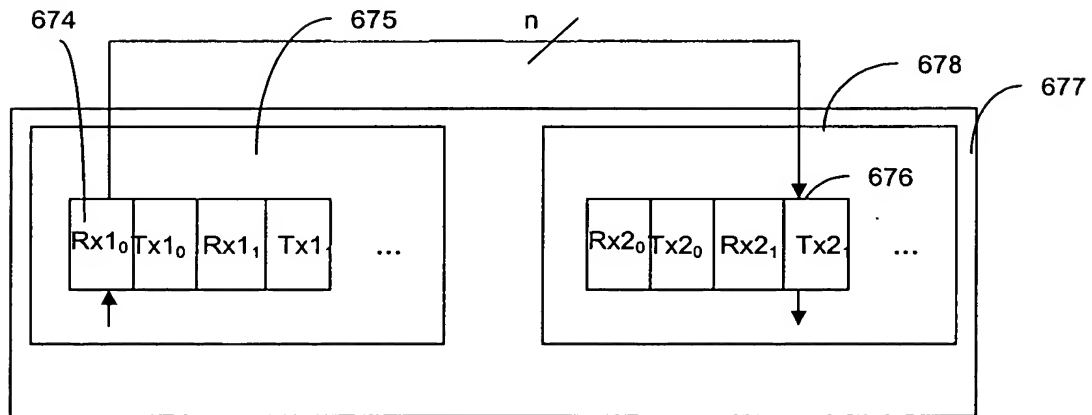
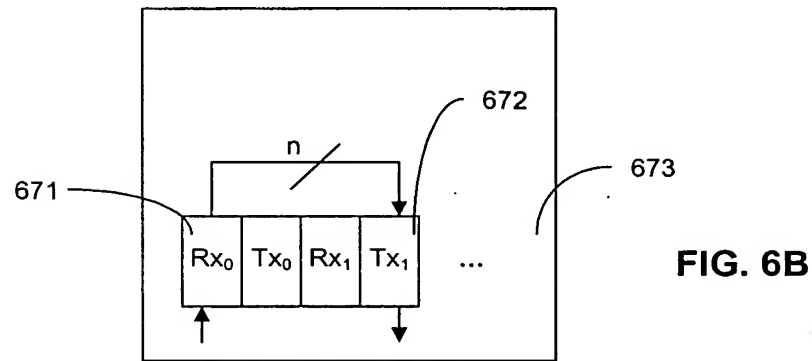
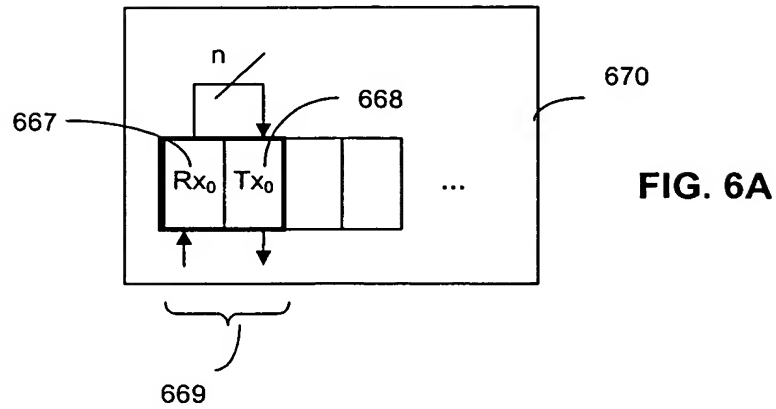


FIG. 6C

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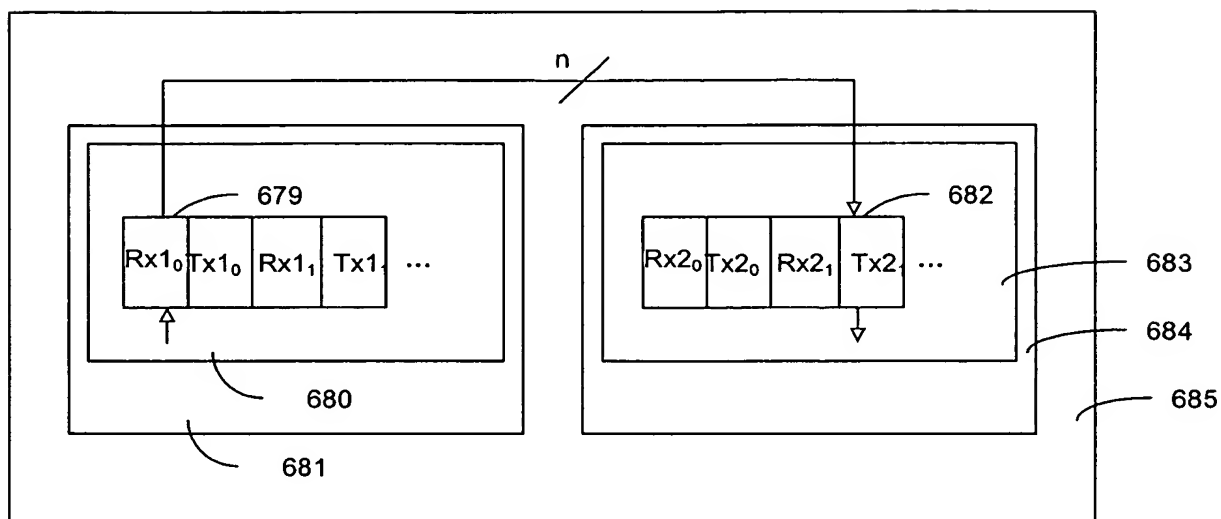


FIG. 6D

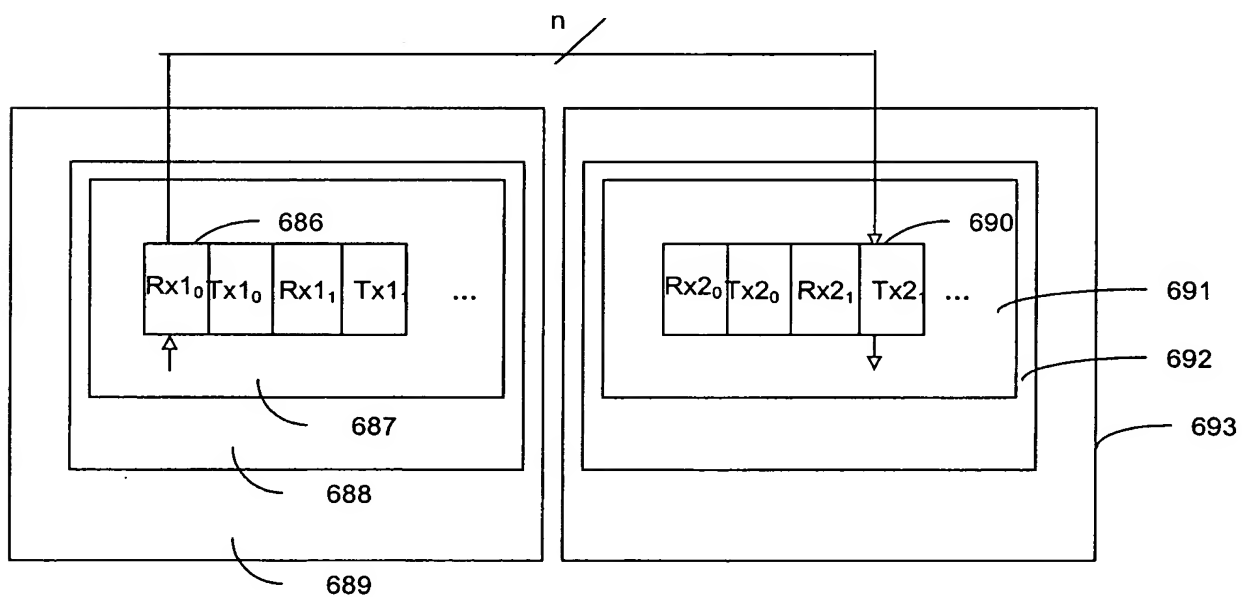
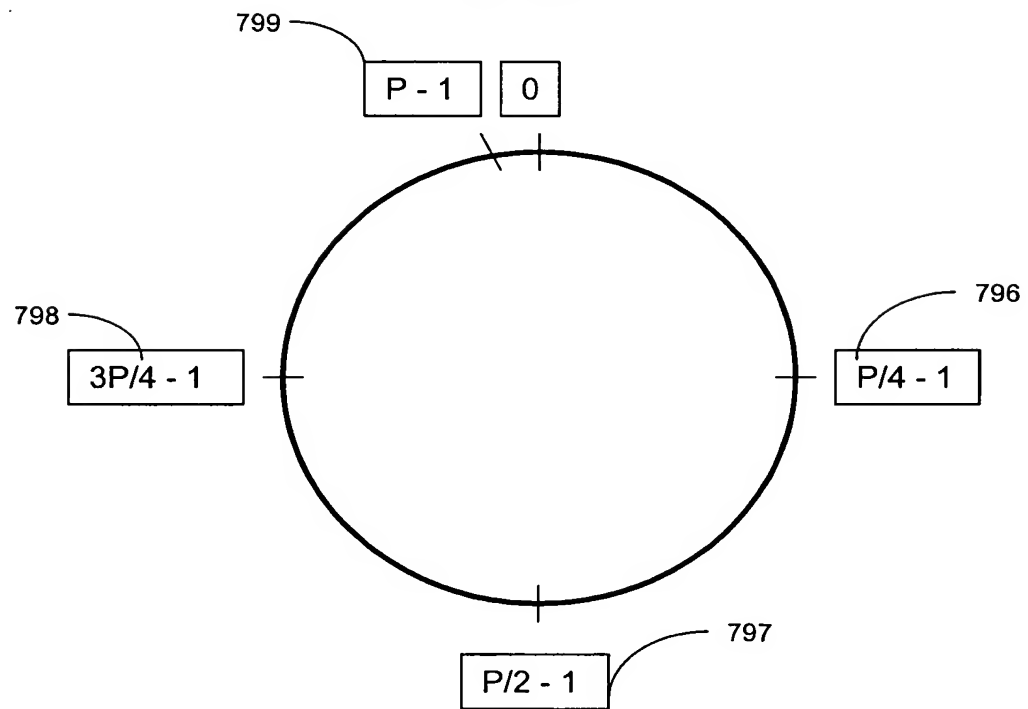
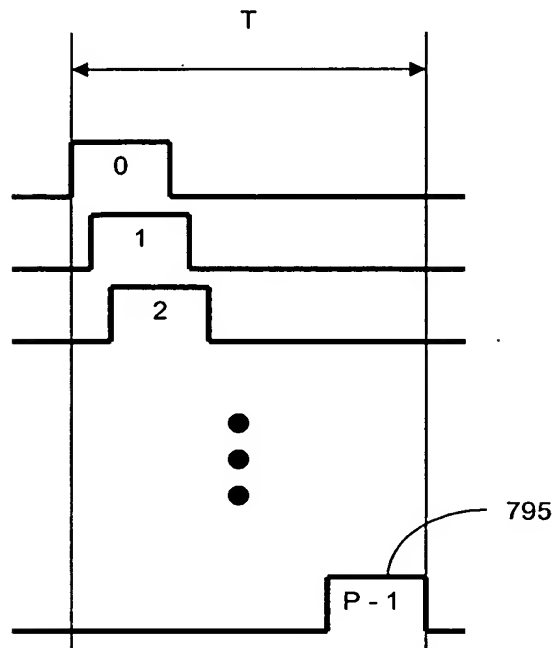
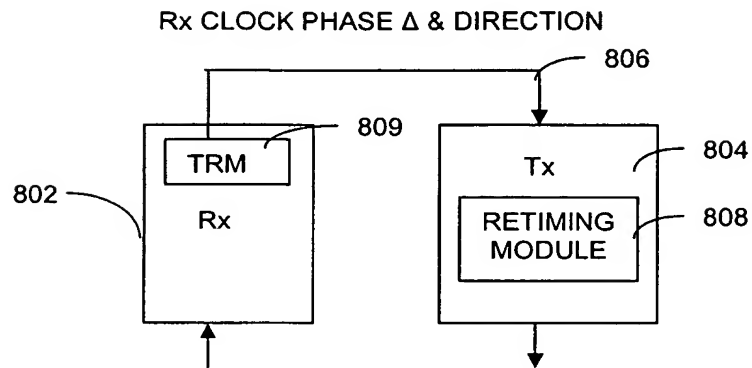


FIG. 6E



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**FIG. 8**

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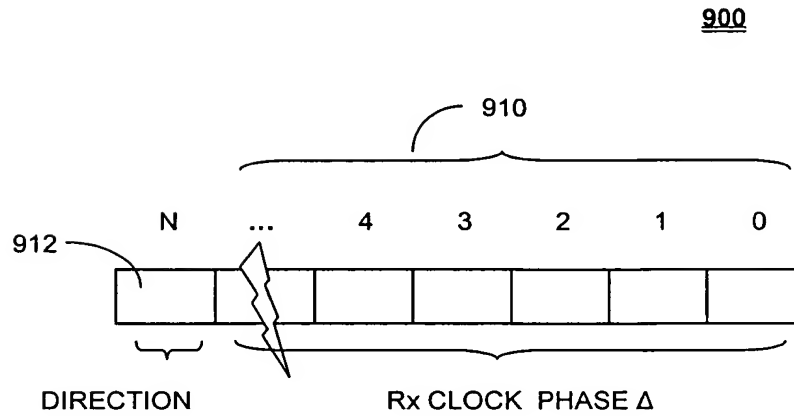


FIG. 9

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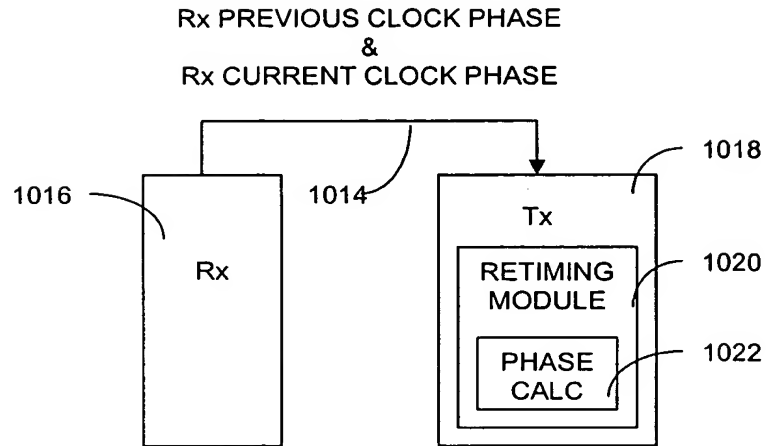


FIG. 10

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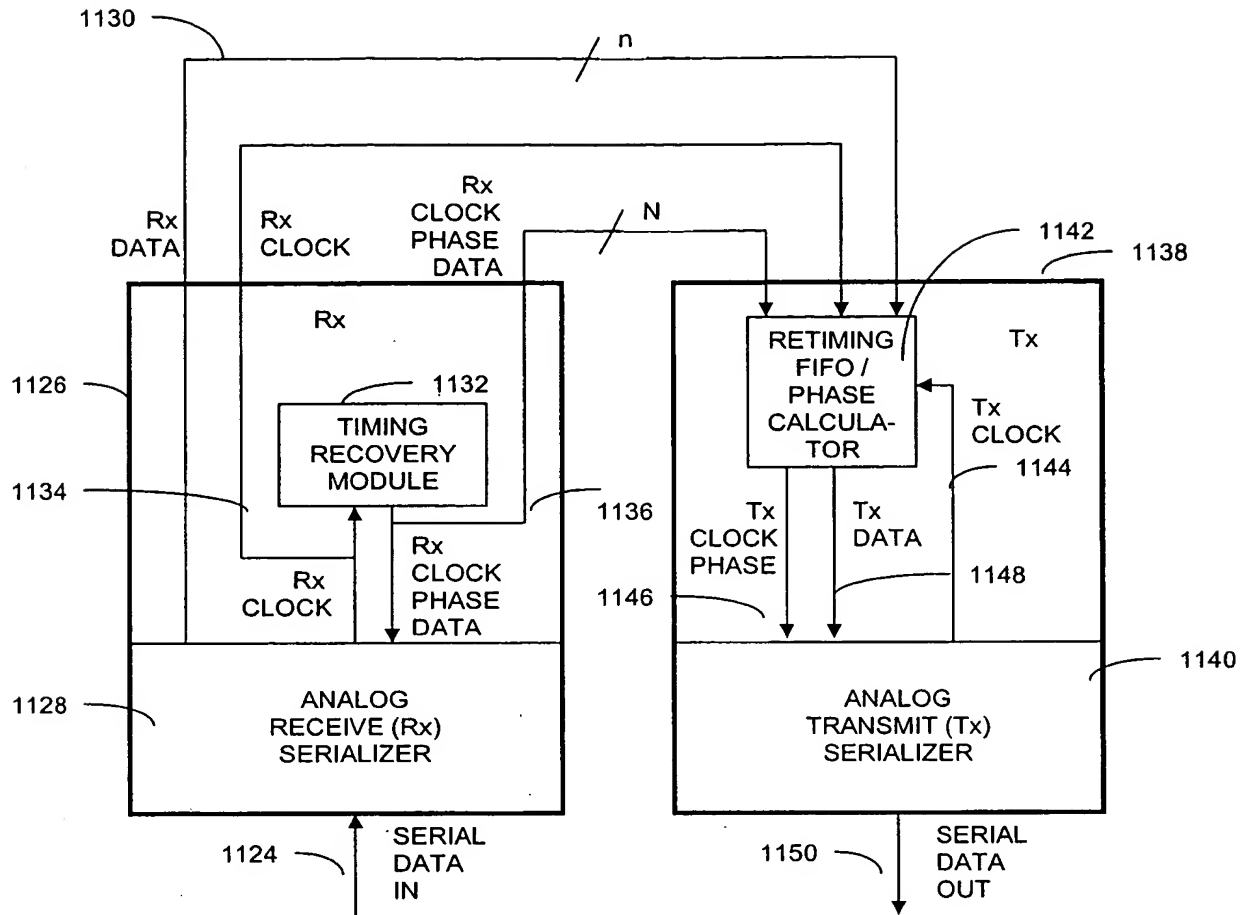


FIG. 11

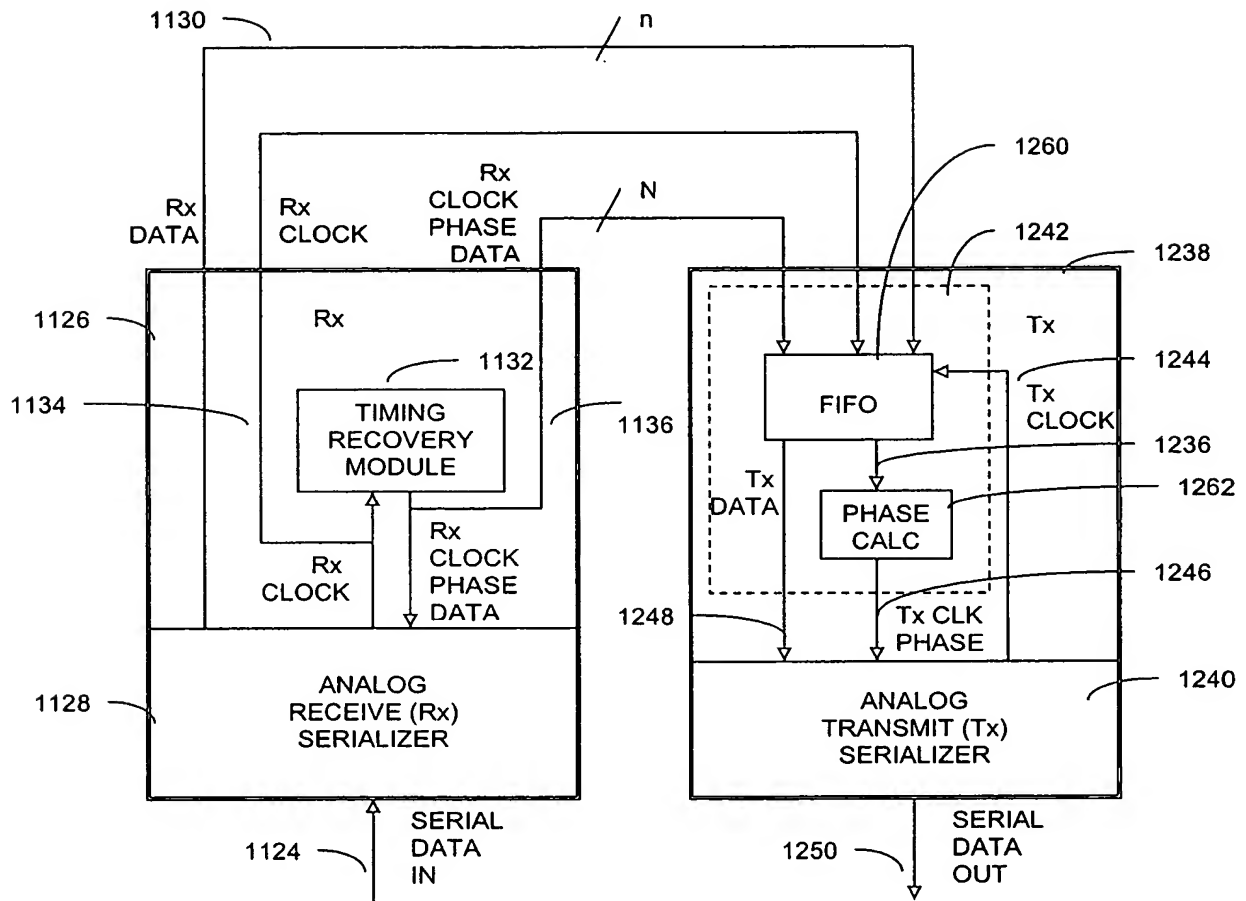


FIG. 12

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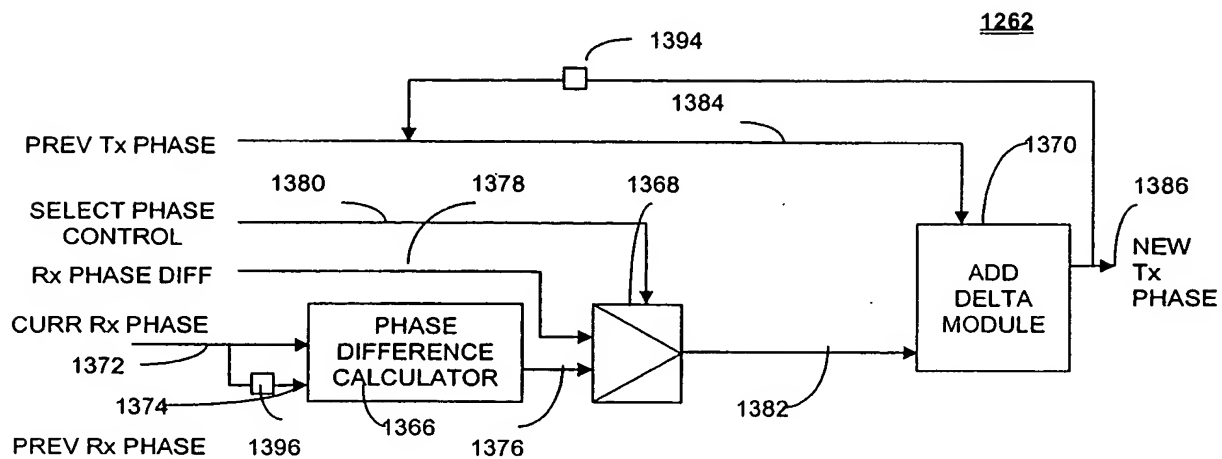


FIG. 13A

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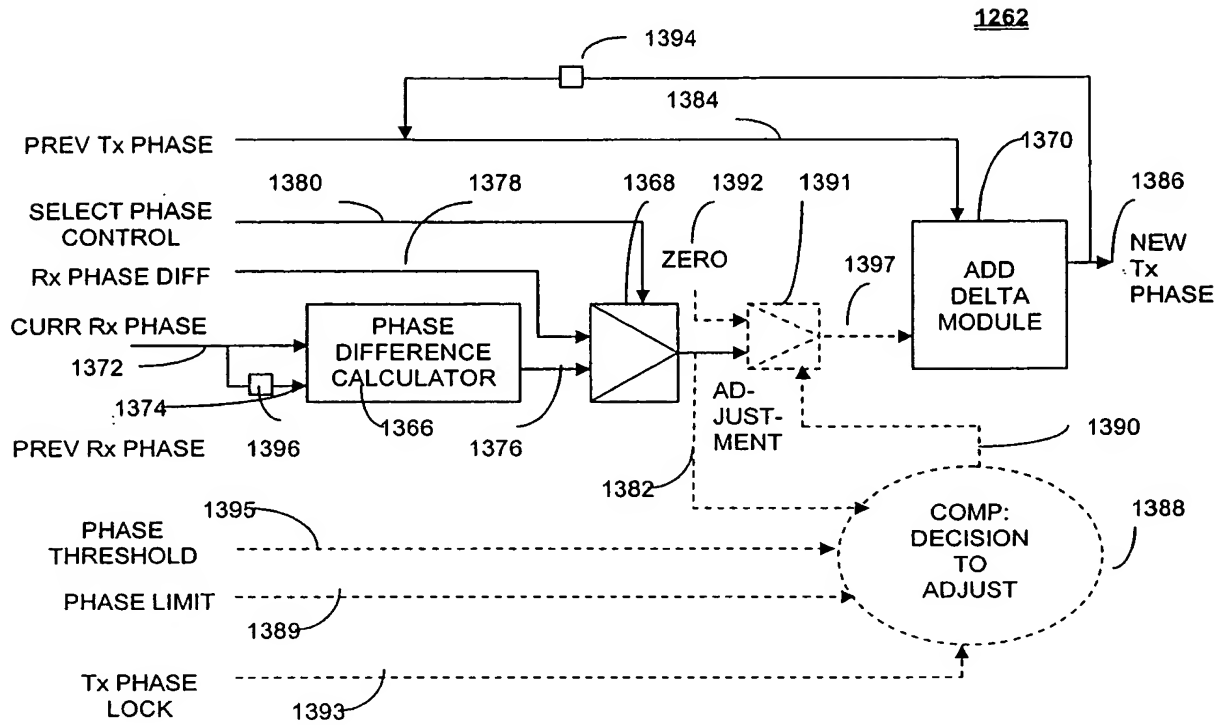


FIG. 13B

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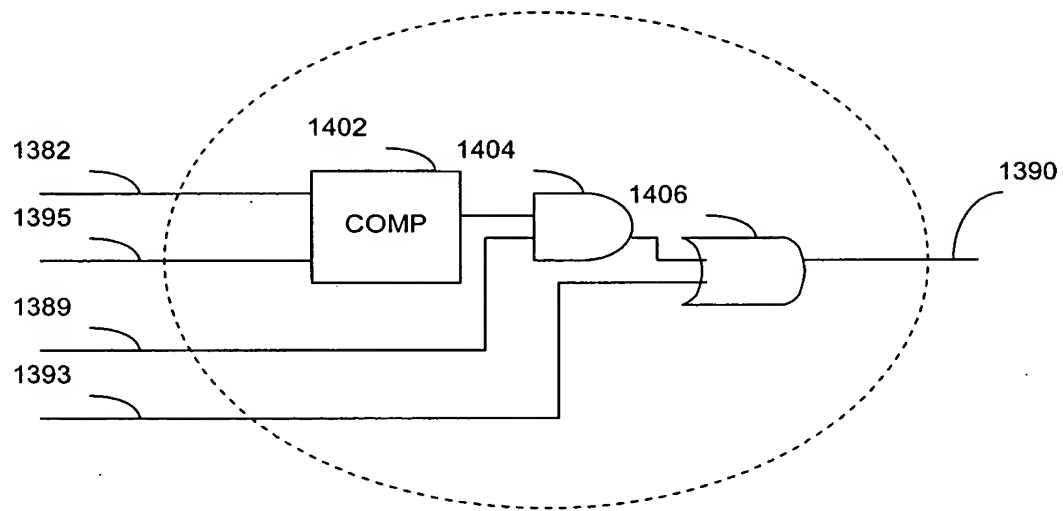
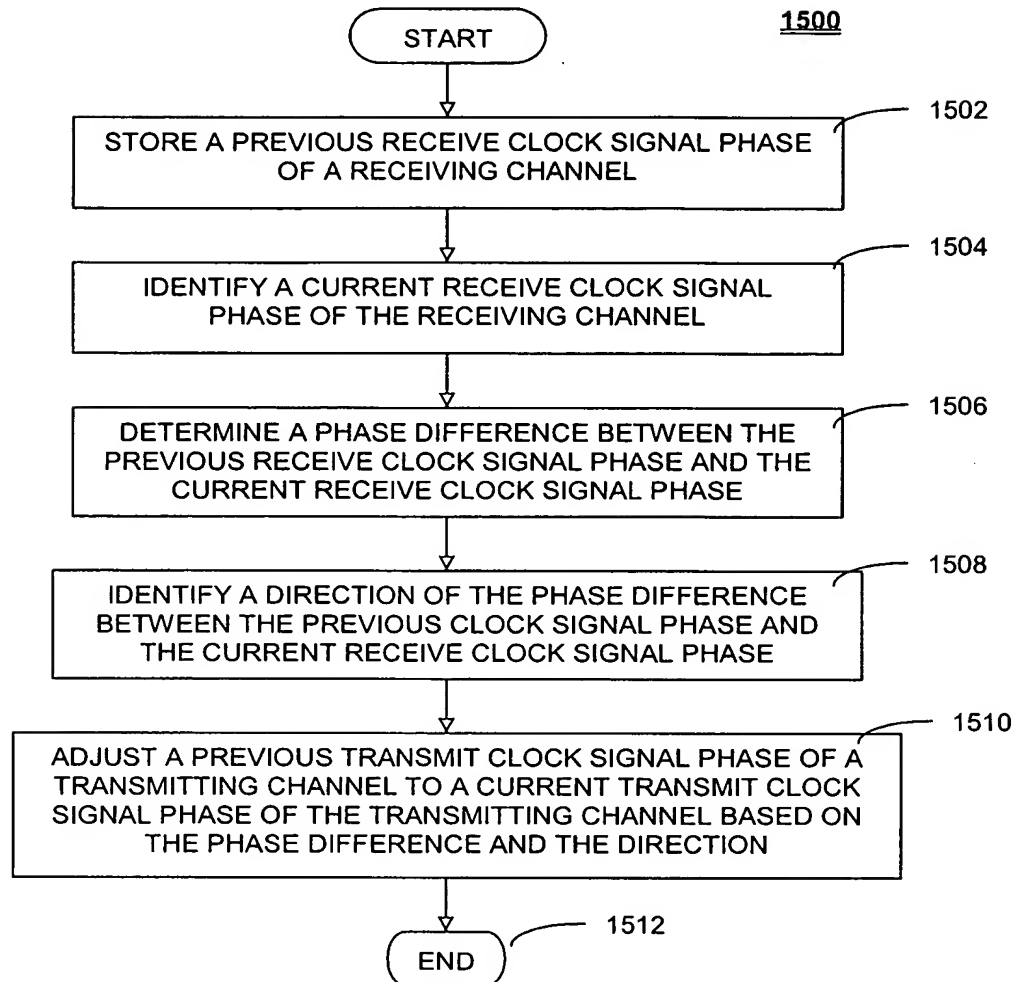


FIG. 14

**FIG. 15**

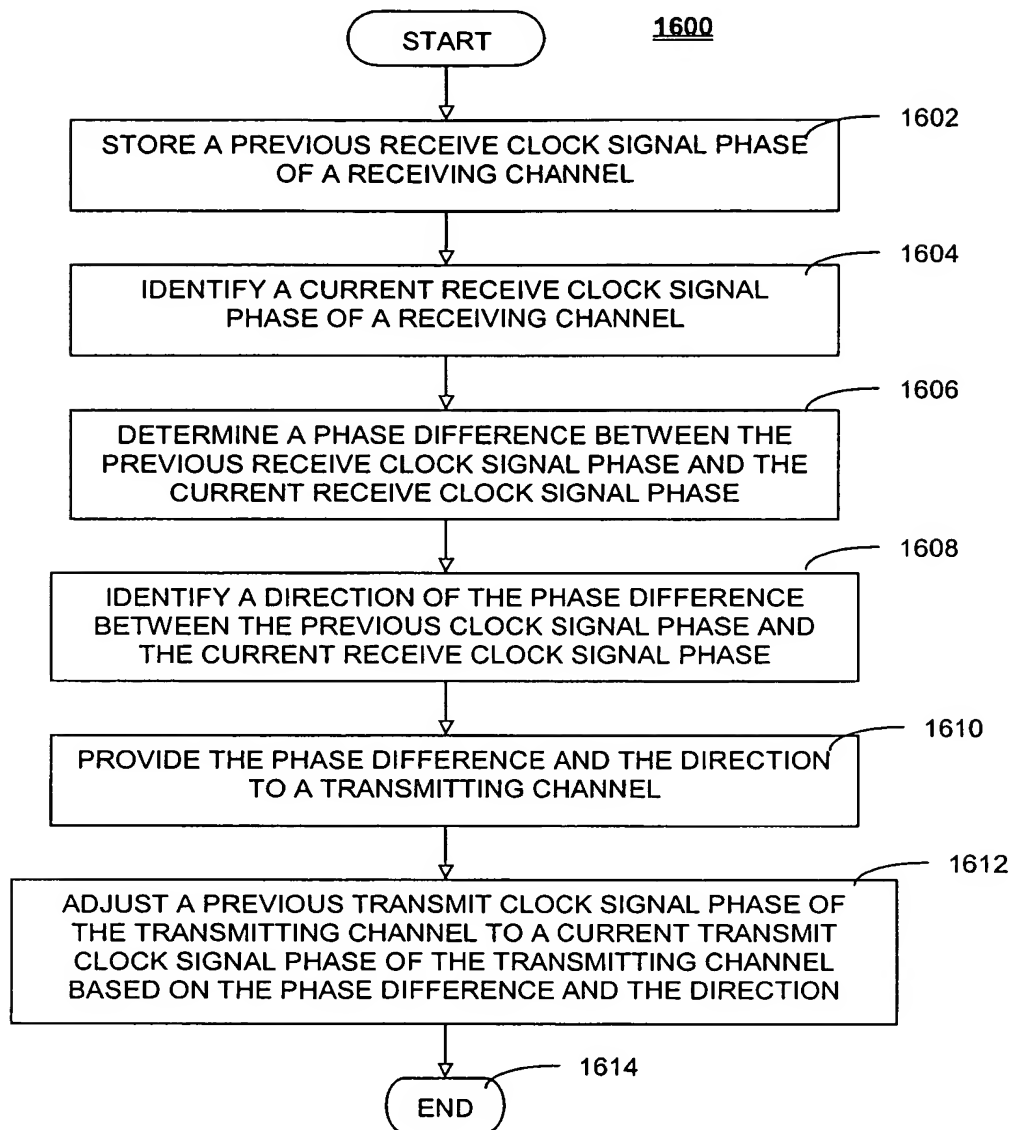
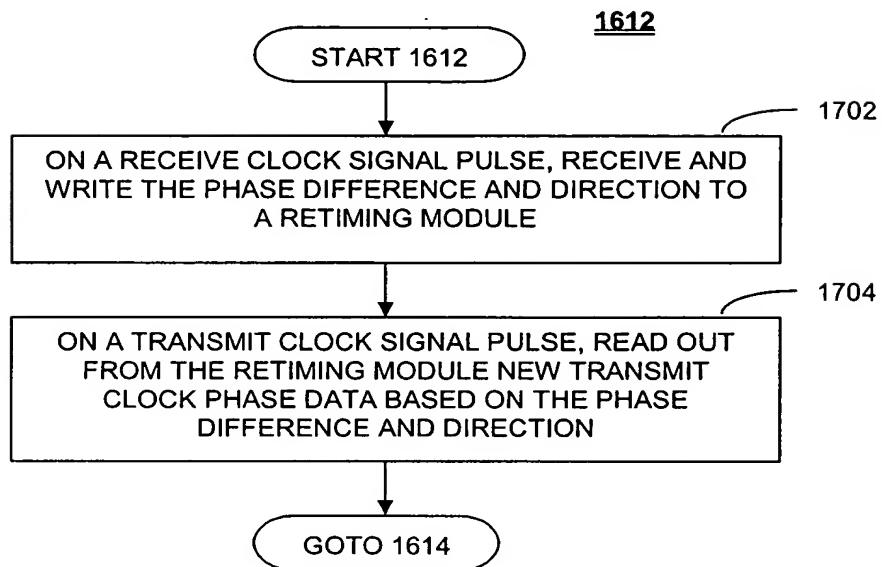


FIG. 16

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**FIG. 17**

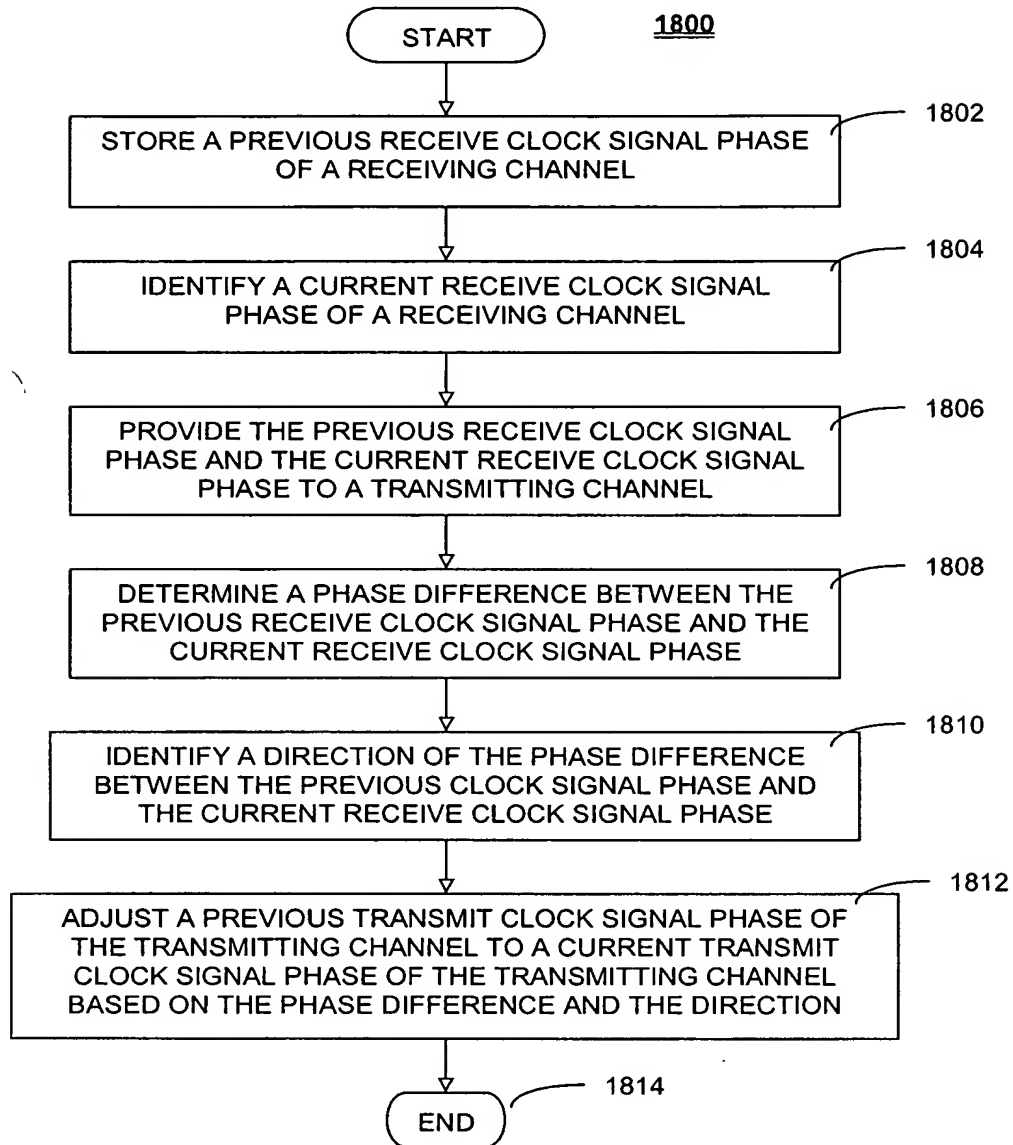


FIG. 18

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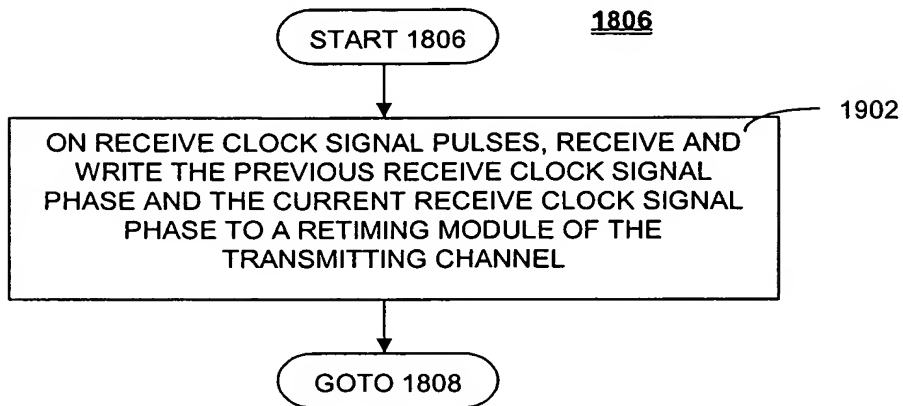


FIG. 19

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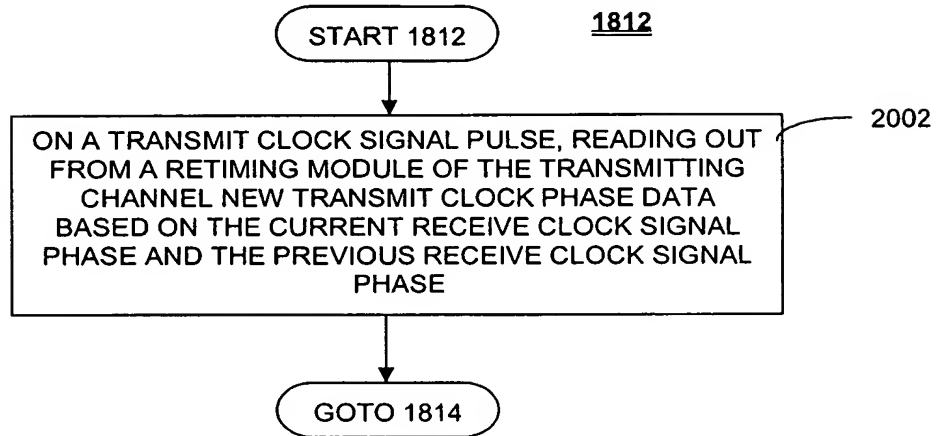
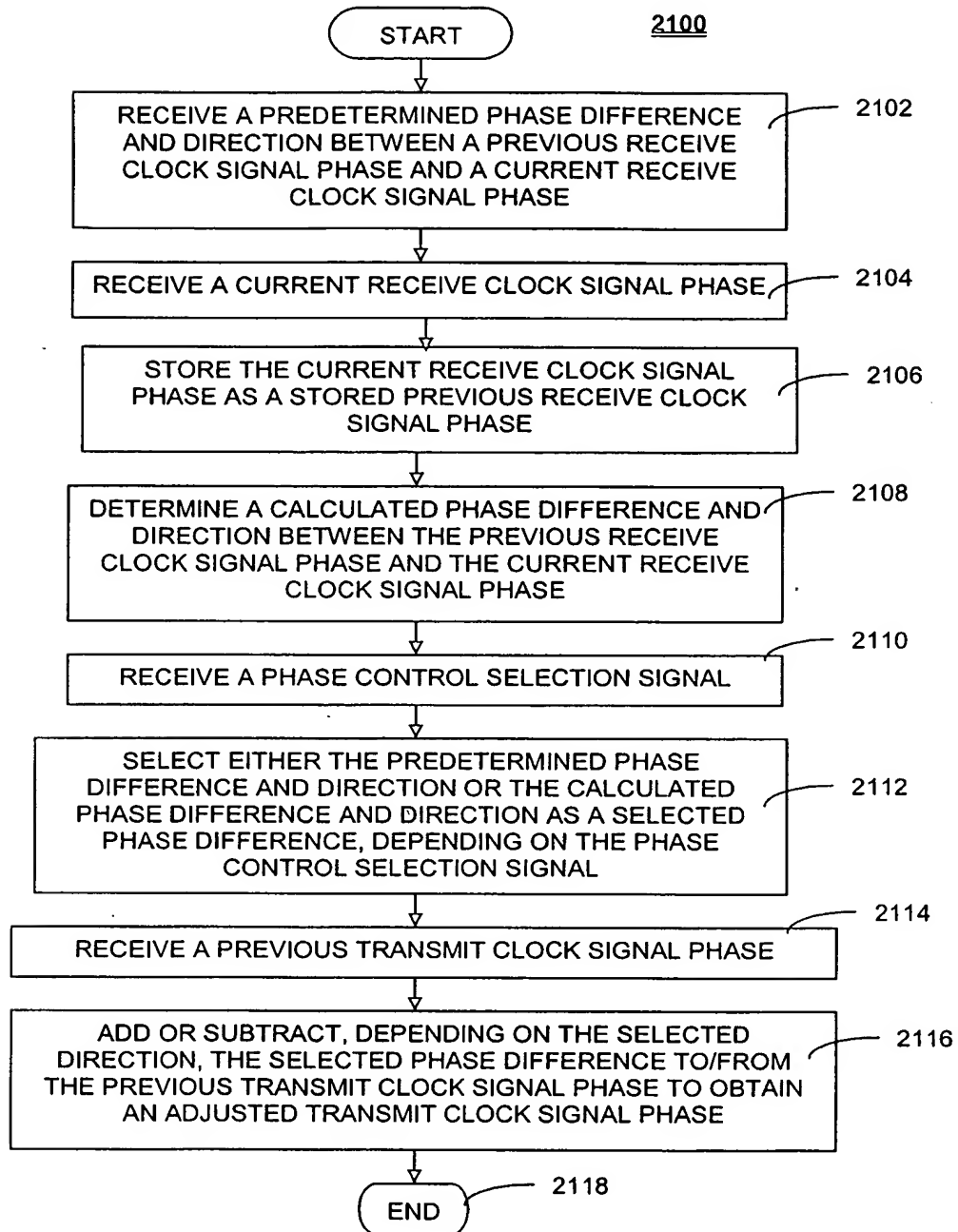


FIG. 20

**FIG. 21**

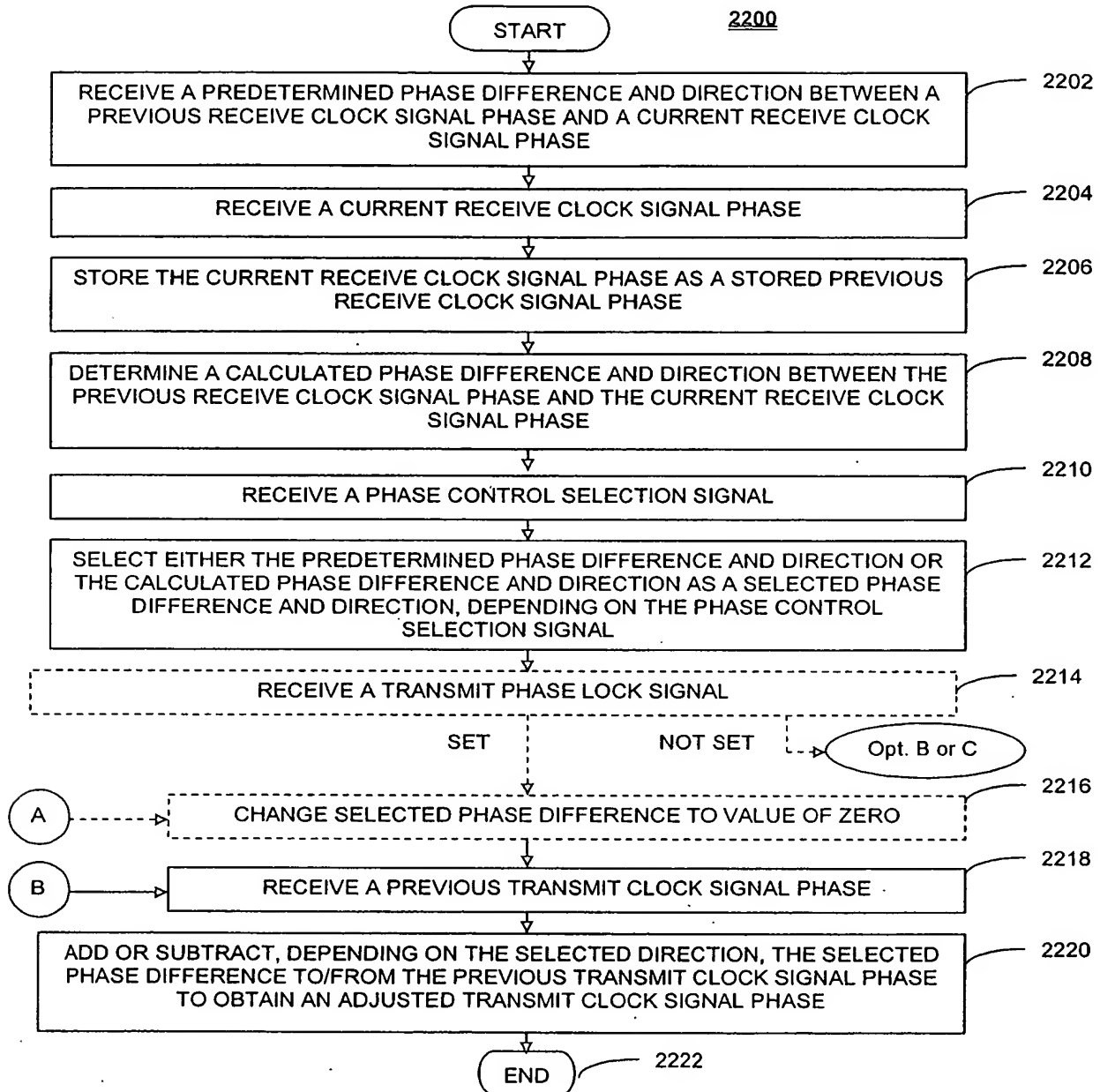


FIG. 22A

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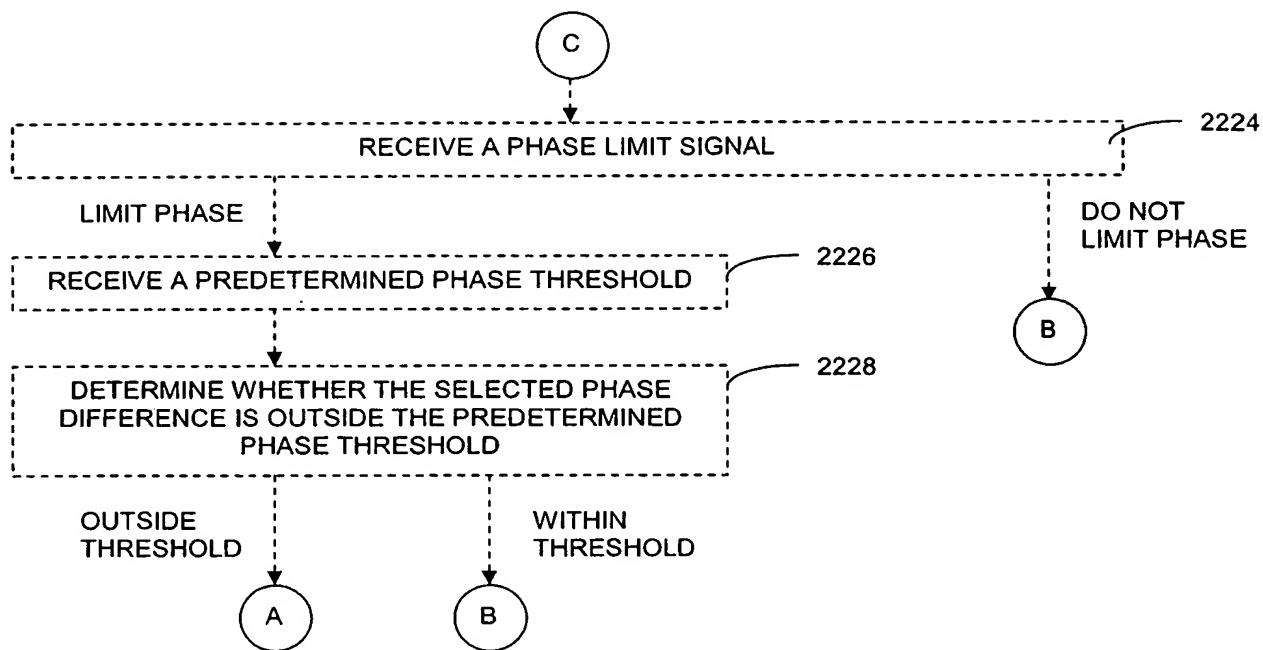
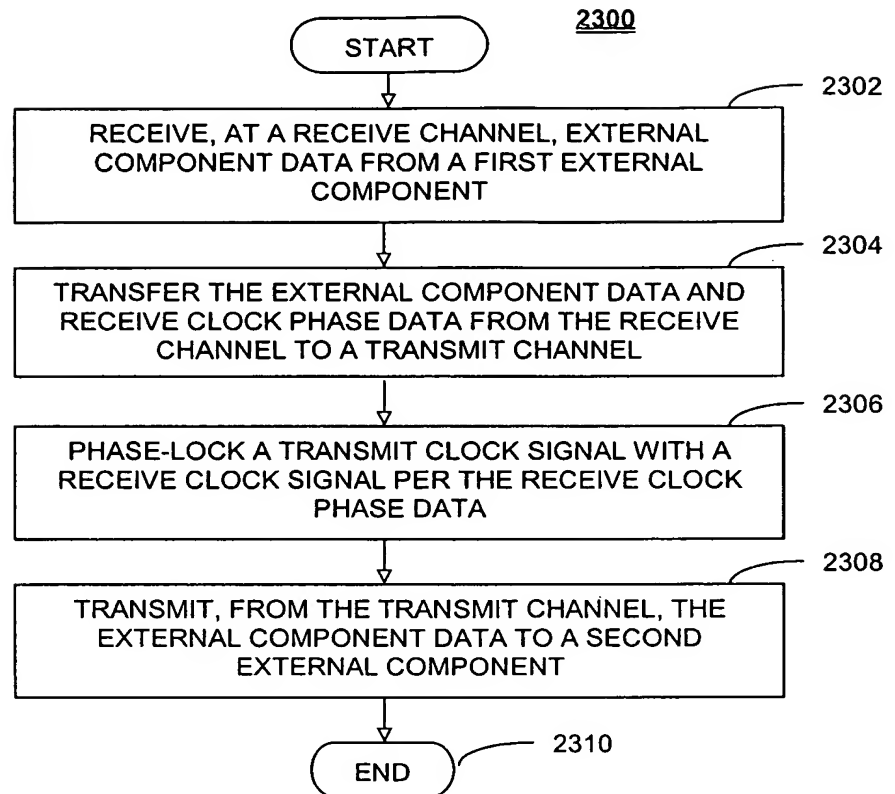


FIG. 22B

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**FIG. 23**